



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,579	03/02/2004	Mohammad H.S. Amin	240105.419C2	6155

500 7590 01/10/2008
SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 5400
SEATTLE, WA 98104

EXAMINER

ARENA, ANDREW OWENS

ART UNIT	PAPER NUMBER
----------	--------------

2811

MAIL DATE	DELIVERY MODE
-----------	---------------

01/10/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/791,579

Applicant(s)

AMIN ET AL.

Examiner

Andrew O. Arena

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 October 2007.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 53-60 and 62-66 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration..
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 53-60 and 62-66 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU2811, TC 2800

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

New grounds of rejection not necessitated by amendment are presented herein, accordingly, this action is non-final. See MPEP § 706.07(a).

Allowable Subject Matter

The indicated allowability of claims 53-59 and 61-64 is hereby withdrawn upon reconsideration of the claim language and of the art of record.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 53-60 and 62-66 are rejected under 35 U.S.C. 102(e) as being anticipated by Zangoskin (US 6,563,311).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by an appropriate showing under 37 CFR 1.131 (see MPEP § 715) or by an appropriate showing under 37 CFR 1.132 (see MPEP § 716).

RE claim 53, Zangoskin discloses a qubit system comprising (e.g., Fig 7):
a plurality of qubits (col 10 ln 60); and
a control system (col 10 ln 50) coupled to each respective qubit in said plurality of qubits, wherein the control system includes:

a bus (ground); and
a plurality of grounding switches (640-N), wherein each grounding switch in the plurality of grounding switches conditionally couples said bus to a respective qubit in said plurality of qubits (col 10 ln 40).

RE claim 54, Zangoskin discloses the control system is configured to entangle the quantum state of two or more qubits in said plurality of qubits (col 10 ln 50).

RE claim 55, Zangoskin discloses said plurality of qubits are arranged in an array (col 10 ln 60) and a qubit in said two or more qubits is not adjacent to any other qubit in said two or more qubits.

RE claim 56, Zangoskin discloses the quantum state of said two or more qubits become entangled (col 10 ln 50) when each respective grounding switch corresponding to said two or more qubits is set so that the two or more qubits are coupled to said bus.
See MPEP § 2114.

RE claim 57, Zangoskin discloses means for reading out a quantum state of one or more qubits in the plurality of qubits (col 10 ln 45).

RE claim 58, Zangoskin discloses means for setting ("freeze" col 10 ln 43) the quantum state of one or more qubits in the plurality of qubits.

RE claim 59, Zangoskin discloses means for entangling the quantum state of one or more qubits in the plurality of qubits (col 10 ln 50).

RE claim 60, Zangoskin discloses a quantum computing system (col 1 ln 13), comprising (e.g., Fig 7):

a plurality of qubits configured in an array (col 10 ln 60), the array having at least one row and at least one column, and wherein each row in the at least one row comprises a linear arrangement of two or more qubits and wherein each column in the at least one column comprises a linear arrangement of two or more qubits (encompassed by “two-dimensional array”); and

a control system coupled to one or more qubits in the plurality of qubits, the control system configured to provide a quantum computing readout current or a quantum computing initialization current to one or more qubits in the plurality of qubits (col 10 ln 39-50); and

a plurality of grounding switches (640-N), wherein each respective grounding switch in the plurality of grounding switches corresponds to a qubit in the plurality of qubits, and wherein each respective grounding switch is configured to conditionally connect the qubit corresponding to the respective grounding switch to a ground.

RE claim 62, Zangoskin discloses (Fig 8) a plurality of current switches (840-N), wherein each respective current switch in the plurality of current switches corresponds to a qubit in the plurality of qubits, and wherein each respective current switch is configured to conditionally connect the qubit corresponding to the respective grounding

switch to a quantum computation readout current or a quantum computation initialization current (col 11 ln 41-45).

RE claim 63, Zangoskin discloses the control system supplies a control voltage (col 10 ln 48) to switchably couple, for each respective qubit in a row of qubits in the array, the current switch and the grounding switch that corresponds to respective qubit to the respective qubit. See MPEP § 2114.

RE claim 64, Zangoskin discloses qubits in the array are grounded by row in the array, the control system further comprising a voltmeter (encompasses col 10 ln 1-20, per MPEP § 2111) coupled between a current switch and a ground of a qubit in the plurality of qubits.

RE claim 65, Zangoskin discloses the control system further comprising means for initializing a column of qubits in the array by providing an initializing current to each qubit in the column (col 10 ln 43 & 60).

RE claim 66, Zangoskin discloses the control system is further configured to readout a quantum state of each qubit in a column of qubits using (col 10 ln 1-20):

means for applying a readout current to each qubit in the column of qubits, and
means for measuring a voltage across each qubit in the column qubits.

See MPEP § 2114.

Response to Arguments


The arguments filed 10/04/2007 have been considered but are moot in view of the new ground of rejection.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Andrew O. Arena
28 December 2007


LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800